

IN THE CLAIMS:

Please find below a listing of all pending claims. The statuses of the claims are set forth in parentheses. For those currently amended claims, underlined emphasis indicates insertions and ~~strikethrough~~ emphasis (and/or double brackets) indicates deletions.

1. (Currently Amended) A synchronous network establishing method of establishing a synchronous network in which a node apparatus conforming to a first synchronization scheme and a node apparatus conforming to a second synchronization scheme co-reside, wherein the first synchronization scheme and the second synchronization scheme implement different synchronous state indication codes for establishing the synchronous network, said method comprising:

receiving a first state indication code used by the first synchronization scheme to indicate a state of a clock signal with respect to each of a plurality of clock signals employed in the first synchronization scheme;

converting the[[a]] first synchronous state indication code used by the first synchronization scheme into a second synchronous state indication code used by the second synchronization scheme when the node apparatus conforming to the second synchronization scheme receives the first synchronous state indication code from the node apparatus conforming to the first synchronization scheme, the second synchronous state indication code being used by the second synchronization scheme to indicate a state of a clock signal with respect to each of the plurality of clock signals employed in the second synchronization scheme.

2. (Previously Presented) The synchronous network establishing method as claimed in claim 1, further comprising:

including the first synchronous state indication code that is supplied from the node apparatus conforming to one of the first scheme and the second scheme in an empty bit of the converted second synchronous state indication code.

3. (Previously Presented) The synchronous network establishing method as claimed in claim 1, further comprising:

using a pre-converted synchronous state indication code included in an empty bit of the first synchronous state indication code that is supplied from the node apparatus conforming to one of the first scheme and the second scheme.

4. (Currently Amended) A node apparatus conforming to a given one of a first synchronization scheme and a second synchronization scheme that is connected to a counterpart node apparatus conforming to the other one of the first synchronization scheme and the second synchronization scheme, wherein the first synchronization scheme and the second synchronization scheme implement different synchronous state indication codes for establishing a synchronous network, said node apparatus comprising:

a receiving unit to receive a synchronous state indication code used by said other one of the first synchronization scheme and the second synchronization scheme to indicate a state of a clock signal with respect to each of a plurality of clock signals employed in said other one of the first synchronization scheme and the second synchronization scheme;

a synchronous state indication code converting unit to convert [[a]]the synchronous state indication code used by said other one of the first synchronization scheme and the second synchronization scheme supplied from the counterpart node apparatus into a synchronous state indication code used by said given one of [[a]]the first synchronization scheme and [[a]]the second synchronization scheme, the synchronous state indication code used by said given one of the first synchronization scheme and the second synchronization scheme being used to indicate a state of a clock signal with respect to each of the plurality of clock signals employed in said given one of the first synchronization scheme and the second synchronization scheme.

5. (Previously Presented) The node apparatus as claimed in claim 4, further comprising:

a selecting unit to select one of the synchronous state indication code supplied from the counterpart node apparatus and the converted synchronous state indication code obtained by the synchronous state indication code converting unit.

6. (Original) The node apparatus as claimed in claim 5, wherein the selecting unit administers switching according to a switching instruction signal.

7. (Previously Presented) The node apparatus as claimed in claim 5, further comprising:

a switch unit to instruct a switching of the selecting unit.

8. (Previously Presented) The node apparatus as claimed in claim 5, further comprising:

a switching instruction unit to detect a bit of a signal supplied from the counterpart node apparatus to determine which of the first scheme and the second scheme said counterpart node apparatus conforms to, and to instruct a switching of the selecting unit based on the determination.

9. (Original) The node apparatus as claimed in claim 4, wherein a content to be converted by the synchronous state indication code converting unit can be arbitrarily changed.